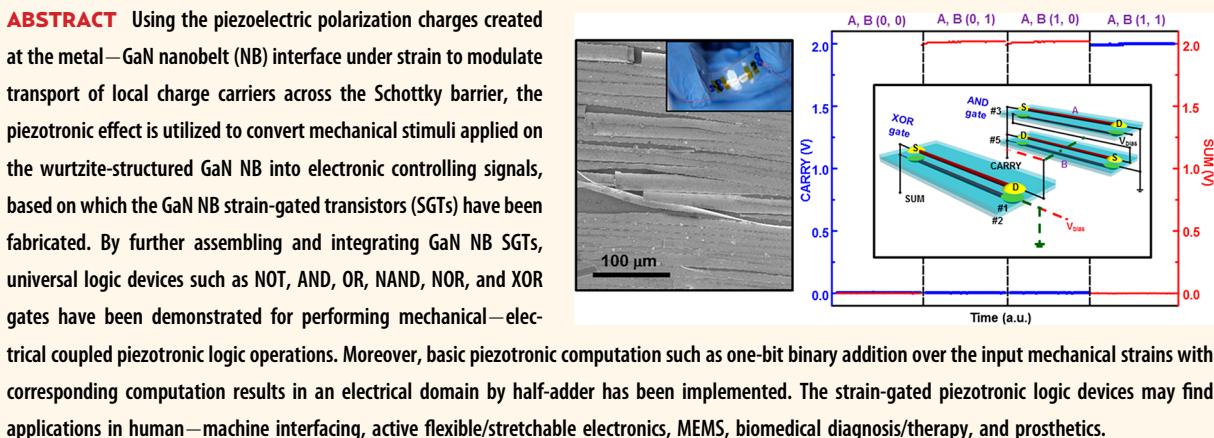


GaN Nanobelt-Based Strain-Gated Piezotronic Logic Devices and Computation

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KEYWORDS: GaN nanobelts · piezotronics · strain-gated transistor · logic nanodevices · logic computation

As the basic components for constructing functional circuits, nanomaterial-based logic devices have attracted numerous interests due to the fact that the miniaturized dimensions of nanomaterials and the ability to modulate compositions in precisely controlled manners can enable properties not available in their bulk counterparts, which might help address some of the critical challenges faced by silicon-based technology.^{1–8} By integrating these logic components with low-power microcontrollers, information storage devices, signal transceivers, ultrasensitive sensors, and embedded energy-scavenging units, self-powered micro/nanosystems (MNS) capable of sustainable and maintenance-free operations can be implemented for applications in environmental monitoring, structure analysis, surveillance, and biomedical diagnosis/therapy.^{9–12} Approaches for developing a direct interface between machine and human/ambient are highly desired for realizing the above applications. Vibration-based mechanical signals are ubiquitous in the environment and provide

the abundant actuation sources to potentially control electronics in MNS.^{13–16} Most existing nanomaterial-based flexible electronics for logic computation and other functions, however, are based on electrically controlled units.^{12,17–19} Efforts are devoted to minimize the effect of substrate strain on performance of these electronic components, which not only requires complicated system integration of heterogeneous components but also lacks proficiency in directly interfacing mechanical actions in an active way that mechanical straining can be utilized to generate new electronic controlling signals. Recently, the nanowire (NW) piezotronic strain-gated transistor (SGT) was introduced^{20,21} based on a two-terminal metal–semiconductor–metal (M–S–M) structure, using the piezoelectric polarization-induced inner-crystal piezopotential in the NW to modulate the charge carrier transport at the contacts without applying the gate voltage as in traditional FET. Consequently, the transport property of a piezotronic SGT is directly controlled by the externally applied force/stress. Most recently, a large-scale

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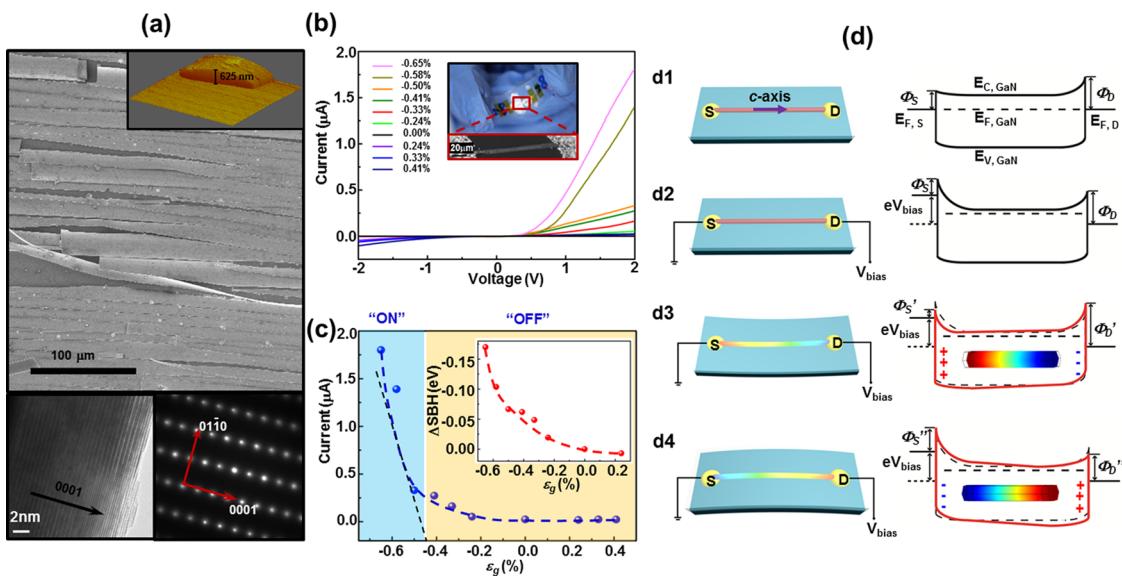


Figure 1. GaN NB piezotronic transistor. (a) SEM image of GaN NBs; HRTEM image of a GaN NB and a corresponding SAED pattern of the same GaN NB. (b) I_{DS} – V_{DS} characteristics of GaN NB piezotronic transistor under different strains. The inset is a digital image and an optical image of a typical piezotronic transistor. (c) I_{DS} – ε_g curve of a typical GaN piezotronic transistor measured at fixed bias of 2 V. The intersection between the x-axis (ε_g) and the black dashed line (tangent of the maximum slope region) indicates that the threshold gate strain ε_t is -0.43% . The inset presents the change of SBH versus applied strains. (d) Band structure of GaN NB piezotronic transistor under different conditions to demonstrate the working principle. The crystallographic c-axis of the NB directs from source to drain as labeled. (d1) Schematic and band structure of a strain-free device, no bias applied. (d2) Schematic and band structure of a strain-free device under bias voltage V_{bias} . (d3) Schematic and band structure of a compressively strained device under bias voltage V_{bias} . (d4) Schematic and band structure of a device under tensile strain and bias voltage V_{bias} .

array of vertical ZnO NW piezotronic transistors has been reported for adaptive and active tactile imaging.²²

Piezotronic effect arises due to the piezoelectric polarization of ions in the crystal. Different from the commonly utilized piezoresistive effect, which is a symmetric volume effect without polarity, the piezotronic effect is an interfacial effect which asymmetrically modulates local contacts/interfaces at different terminals of the device.^{14,15} Piezotronic effect is universal, as well, which is not only evident in n-type nanowire materials but also exists in piezoelectric semiconductor materials of different doping types and morphologies (such as thin films).^{23,24} Wurtzite-structured GaN, similar to ZnO, is also a candidate material for investigating piezotronic effect.^{25,26} In this study, GaN nanobelt (NB) SGTs have been fabricated by using the piezoelectric polarization charges created at the metal–GaN NB interface under strains to modulate transport of local charge carriers across the Schottky barrier, in which the mechanical stimuli applied on wurtzite-structured GaN NBs are converted into electronic controlling signals. By further assembling and integrating GaN NB SGTs, universal logic devices such as NOT, AND, OR, NAND, NOR, and XOR gates have been demonstrated for performing mechanical–electrical coupled piezotronic logic operations. Moreover, basic piezotronic computation such as one-bit binary number addition by half-adder has been demonstrated.

RESULTS AND DISCUSSION

GaN NBs were derived by strain-controlled cracking of thin solid GaN films.²⁷ The as-obtained GaN NBs are well-separated with lengths of several hundred micrometers, widths of $\sim 10\ \mu\text{m}$, and thicknesses of $\sim 625\ \text{nm}$, manifesting the anisotropic belt morphology (Figure 1a, top). The single crystallinity of the GaN NB has also been confirmed, and its polar c-axis is determined to lie in the longitudinal direction of the NB, as shown by a high-resolution transmission electron microscopy (HRTEM) image and corresponding selected area electron diffraction (SAED) pattern in Figure 1a. The piezotronic SGT was fabricated by transferring and bonding an individual GaN NB laterally on the polystyrene (PS) film substrate ($\sim 500\ \mu\text{m}$ thick), with its c-axis in the substrate plane. Two ends of the NB were fixed by silver paste, which also served as source and drain electrodes, to form an M–S–M structure. A thin layer of polydimethylsiloxane was used to package the device, which not only enhanced the mechanical robustness of the whole device but also prevented the degradation of the GaN NB by gas or moisture in the environment. The optical images of an as-fabricated GaN NB piezotronic SGT is shown in Figure 1b (inset).

Once the substrate was bent, a tensile/compressive strain was created in the NB because the mechanical behavior of the entire structure was determined by the substrate.^{19,20} I_{DS} – V_{DS} characteristic for a single GaN

NB SGT was obtained as a function of the strains induced in the SGT (Figure 1b), which exhibited the asymmetric trend in current response to strains at source and drain electrodes, as dictated by piezotronic effect. For piezotronic SGT, the applied mechanical strains produce the piezopotential which can effectively change the Schottky barrier height (SBH) at the metal–semiconductor (M–S) contact and thus function as the controlling input signal to gate/modulate the electrical transport in the SGT. The magnitude and the sign of applied strains can be calculated following the method reported elsewhere.^{20,21} The I_{DS} – ε_g curve of a typical GaN NB SGT measured at a fixed bias of 2 V (Figure 1c) shows that I_{DS} decreases as the strain gate ε_g increases (the tensile/compressive strains are defined as positive/negative, respectively), and the threshold gate strain ε_T is determined as -0.43% . The I – ε_g transfer curve determined at a bias voltage of 2 V (Supporting Information Figure S1) indicates that the as-fabricated GaN NB SGT had a peak pseudo-transconductance ($g_m = |dI|/d\varepsilon_g$) of $10 \mu\text{A}$ for a strain change of $\Delta\varepsilon_g = 1\%$. The I_{on} and I_{off} of the SGTs can be determined as 1.8 and $0.0188 \mu\text{A}$, respectively, at $\varepsilon_{g(on)} = \varepsilon_T - 0.2\%$ and $\varepsilon_{g(off)} = \varepsilon_T + 0.8\%$, so that 20% of the ε_g swing below the threshold strain ε_T turns the piezotronic transistor on, while 80% defines the “off” state, as illustrated in Figure S1. The corresponding I_{on}/I_{off} ratio of 95.7 is comparable to previously reported values from semiconductor nanowire-based FET driven by electrical signals and piezotronic SGTs based on ZnO NWs.^{17,21}

The working principle of the GaN NB SGTs is explained using band diagrams shown in Figure 1d. A strain-free GaN NB SGT formed Schottky contacts of different barrier heights (Φ_S and Φ_D) with metal electrodes at both ends (Figure 1d1). The transport characteristics of the M–S–M structure-based SGT devices are dictated by the reverse biased Schottky contact. When the drain was forward biased, the quasi-Fermi levels at the source ($E_{F,S}$) and the drain ($E_{F,D}$) were separated by an amount of eV_{bias} , where V_{bias} corresponds to the applied bias (Figure 1d2). Once a strain was applied onto the GaN NB, distribution of piezopotential was induced along the c -axis, with its polarity depending on the sign of the strain (Figure 1d3,d4).²⁸ A negative piezopotential at the semiconductor side effectively increases the local SBH, while a positive piezopotential reduces the barrier height. When the GaN NB SGT was under compressive strain (Figure 1d3), SBH at the reverse biased source contact was reduced by the strain-induced positive piezopotential, which gave rise to an increased current in the device and hence the “on” state. Alternatively, by changing the compressive strain to tensile, as shown in Figure 1d4, SBH at the reverse biased source contact was now increased by the strain-induced negative piezopotential, resulting in the decreased current and the

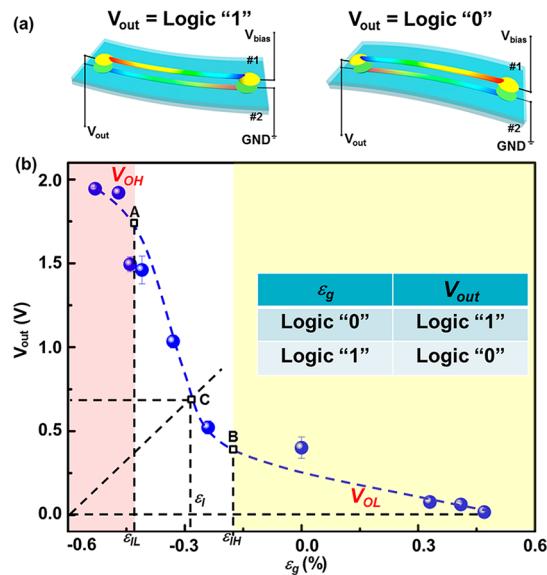


Figure 2. GaN NB piezotronic inverter. (a) Schematics of a GaN piezotronic inverter performing logic operations in response to the strain inputs, which is defined as strains applied on #2 SGT. Mechanical strain input logic “0” indicates that #1 SGT is “on” and #2 SGT is “off”, hence the electrical output is logic “1”. Mechanical strain input logic “1” indicates that #1 SGT is “off” and #2 SGT is “on”, leading to the electrical output logic “0”. The c -axis direction is the same as defined in Figure 1. (b) Strain–voltage transfer characteristic (SVTC) and noise margins of the GaN NB piezotronic inverter at a fixed bias of 2 V. The slope of the black dashed line connecting the origin and point C is 1; the slopes of the tangent at points B and C are both -1 . Inset presents the truth table of a piezotronic inverter.

“off” state. Therefore, by changing the externally applied strains from compressive to tensile, the electrical output of piezotronic SGTs can be tuned from “on” to “off”. The role played by piezopotential was to effectively change the local contact characteristics through an internal field which depends on the crystallographic orientation of the material and the sign of the strain. The changes in SBH under different strains can be derived as²⁰

$$\ln[I(\varepsilon_g)/I(0)] = -\Delta\Phi_S/kT \quad (1)$$

where $I(\varepsilon_g)$ and $I(0)$ are the currents measured through the SGT at a fixed bias with and without applied strains, respectively. The corresponding $\Delta\Phi_S$ – ε_g curve clearly presents the modulation effect of strains on contact characteristics (Figure 1c).

The GaN NB-based piezotronic logic gates can be realized by assembling GaN NB SGTs. Figure 2a shows the schematic of a GaN NB piezotronic inverter (NOT gate). Two GaN NB SGTs were packaged on the top and bottom surfaces of the same flexible substrate. By defining the strain applied on the #2 SGT (the bottom one) as the mechanical logic input of this inverter, an experimental truth table and strain–voltage transfer characteristic (SVTC) for the piezotronic strain-gated inverter can be obtained (Figure 2b). When the inverter was bent upward (left part of Figure 2a), a compressive

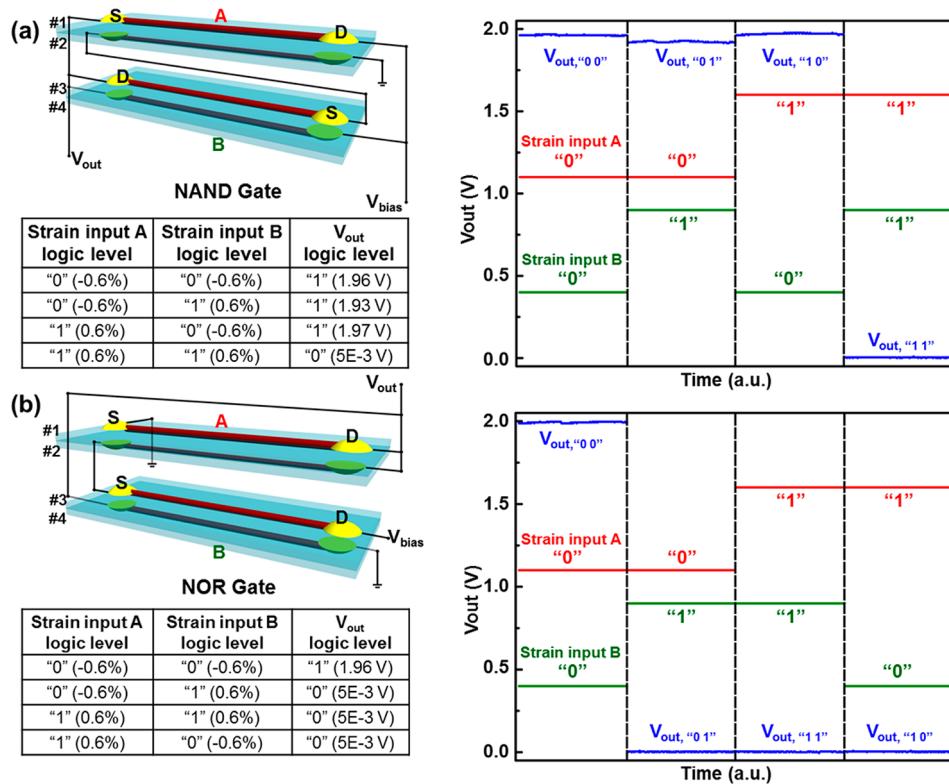


Figure 3. GaN NB piezotronic NAND and NOR logic gates. (a) Schematic of the GaN NB piezotronic NAND gate. Strain input A is defined as strains applied to #2 SGT; strain input B is defined as strains applied to #3 SGT. Experimental truth table is presented with physical values following each corresponding logic level. The right part shows the measured electrical output voltages of NAND gate *versus* the mechanical input strains. Blue lines are the electrical output voltages of NAND gate; red and green lines represent the mechanical strain input applied on inverters A and B, correspondingly. (b) Schematic of the GaN NB piezotronic NOR gate. Strain input A is defined as strains applied to #1 SGT; strain input B is defined as strains applied to #4 SGT. Experimental truth table is presented with physical values following each corresponding logic level. The right part shows the measured electrical output voltages of the NOR gate *versus* the mechanical input strains. Blue lines are the electrical output voltages of the NOR gate; red and green lines represent the mechanical strain input applied on inverters A and B, correspondingly.

strain of -0.6% was induced in the #1 transistor, while a tensile strain of the same magnitude was simultaneously created in the #2 transistor, which led to the complementary “on” and “off” states in #1 and #2 SGTs, respectively. In this case, an electrical logic “1” output (high voltage output) could be observed. On the other hand, if the inverter was bent downward, as shown in the right part of Figure 2a, the #1 SGT was now turned “off” and the #2 SGT was “on”, with an electrical logic “0” output (low voltage output) observed. The GaN piezotronic strain-gated inverter therefore functions in a similar way to the conventional complementary metal oxide semiconductor (CMOS) inverters and performs logic inversion operation between mechanical and electrical domains.

The SVTC and noise margins²¹ of the GaN NB piezotronic inverters were obtained by plotting the measured output voltages *versus* the applied external strains, as shown in Figure 2b. V_{OH} and V_{OL} represent the high and low output voltage of the piezotronic inverter, with theoretical values of $V_{OH} = V_{bias} = 2\text{ V}$ and $V_{OL} = 0\text{ V}$. Here, the experimental values of V_{OH} and V_{OL} are 1.94 and 0.017 V, respectively. The difference between experimental and theoretical values was probably caused by the voltage drop across the SGT

device which was “on” during the measurement. The logic swing of the piezotronic inverter is defined as $V_{OH} - V_{OL} = 1.92\text{ V}$. The switching threshold strain of the piezotronic inverter ε_I , at which the electrical output of the inverter switches between logic “1” and “0” states, is determined at point C with a corresponding strain value of -0.29% (Figure 2b). The numerical value for slope of the dashed line connecting the origin and point C is 1. In order to characterize the effect of mechanical input (strain gating signal) on the electrical output of the inverter, two positions where the numerical value for the slope of the SVTC curve equals -1 are labeled as points A and B (Figure 2b). Points A ($\varepsilon_{IL} = -0.44\%$) and B ($\varepsilon_{IH} = -0.17\%$) represent the largest input strain corresponding to output logic “1” and the smallest input strain corresponding to output logic “0”, respectively. When the applied strain lies within the region where $\varepsilon < \varepsilon_{IL}$ (pink zone in Figure 2b), the electrical output of the inverter is logic “1”; when the applied strain lies within the region where $\varepsilon > \varepsilon_{IH}$ (yellow zone in Figure 2b), the electrical output of the inverter is logic “0”. In the logic low mechanical input region, #1 SGT is “on” and #2 SGT is “off”, while in the logic high mechanical input region, #1 SGT is “off” and #2 SGT is “on”.

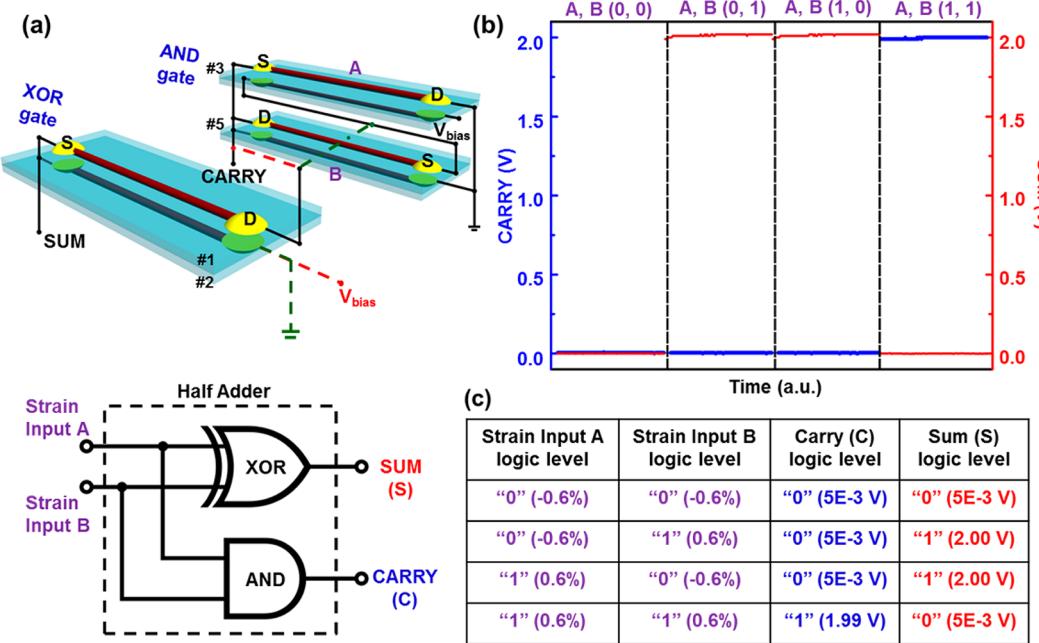


Figure 4. GaN NB piezotronic half-adder. (a) Schematics of GaN NB piezotronic half-adder by integrating one piezotronic XOR gate and one piezotronic AND gate. (b) Measured electrical output voltages of the half-adder. Blue lines represent the CARRY output; red lines represent the SUM output. The symbol “A, B (0, 1)” means mechanical strain input A is logic “0” and mechanical strain input B is logic “1”; the rest are defined in a similar way. (c) Experimental truth table of GaN NB piezotronic half-adder, with physical values following the corresponding logic levels.

More universal piezotronic logic operations can be achieved by systematically integrating GaN NB piezotronic inverters which are gated individually by separate strain inputs. Figure 3a,b shows the schematics of the GaN NB piezotronic NAND gate and NOR gate, respectively, by connecting two GaN NB piezotronic inverters properly in each case. The measured electrical output voltages of the NAND gate (NOR gate) *versus* the mechanical input strains are plotted in the right part of Figure 3a (3b). Blue lines are the experimentally measured electrical output voltages of the NAND gate (NOR gate), while red and green lines represent the logic levels of input mechanical strains applied on inverters A and B, respectively. The physical values of the output and input signals are listed in the experimental truth tables in Figure 3. The strain input A was defined as the strain applied on the #2 SGT in the NAND gate and the #1 SGT in the NOR gate, while the strain input B was defined as the strain applied on the #3 SGT in the NAND gate and the #4 SGT in the NOR gate. In a similar manner, piezotronic strain-gated AND gate, OR gate, and XOR gate have also been realized by integrating piezotronic inverters. The corresponding schematics and experimental results for these piezotronic logic gates are presented in Figures S2–S4, respectively.

By further integrating two different piezotronic strain-gated logic gates in a specific way, the piezotronic logic computation based on GaN NBs was demonstrated, which performed arithmetic operations over mechanical signals and provided corresponding electrical outputs. Figure 4a presents the schematic of a piezotronic

strain-gated one-bit half-adder, which consists of a piezotronic XOR gate and a piezotronic AND gate. The strain input for the piezotronic XOR gate and the strain input for inverter B in the piezotronic AND gate were unified and noted as strain input B for the half-adder (Figure 4); the electrical complementary input for the XOR gate and the strain input for inverter A in the piezotronic AND gate were unified and noted as strain input A for half-adder (Figure 4). The unification of two strain inputs into strain input B for the half-adder is straightforward by defining the strain applied to #2 SGT in the XOR gate and #5 SGT in the AND gate as the strain input B. To unify the electrical complementary input for the XOR gate and the strain input for inverter A in the AND gate, input V_A of the XOR gate (same definition as mentioned for the XOR gate in Figure S4) needed to be unified with strains applied to #4 SGT in the AND gate, which was defined as strain input A of the half-adder. When the mechanical strain input A of the half-adder was logic “0”, the XOR gate was connected to the AND gate by the red dashed lines, as shown in Figure 4a; when the mechanical strain input A was logic “1”, the XOR gate was connected to the AND gate by the green dashed lines, as shown in Figure 4a. It is in this way that the electrical complementary input for the XOR gate and the mechanical strain input for the AND gate were unified into one mechanical input and kept consistent to each other to perform addition computations in a similar manner to the conventional electrically controlled half-adder. Two measured electrical outputs of the piezotronic half-adder, labeled as

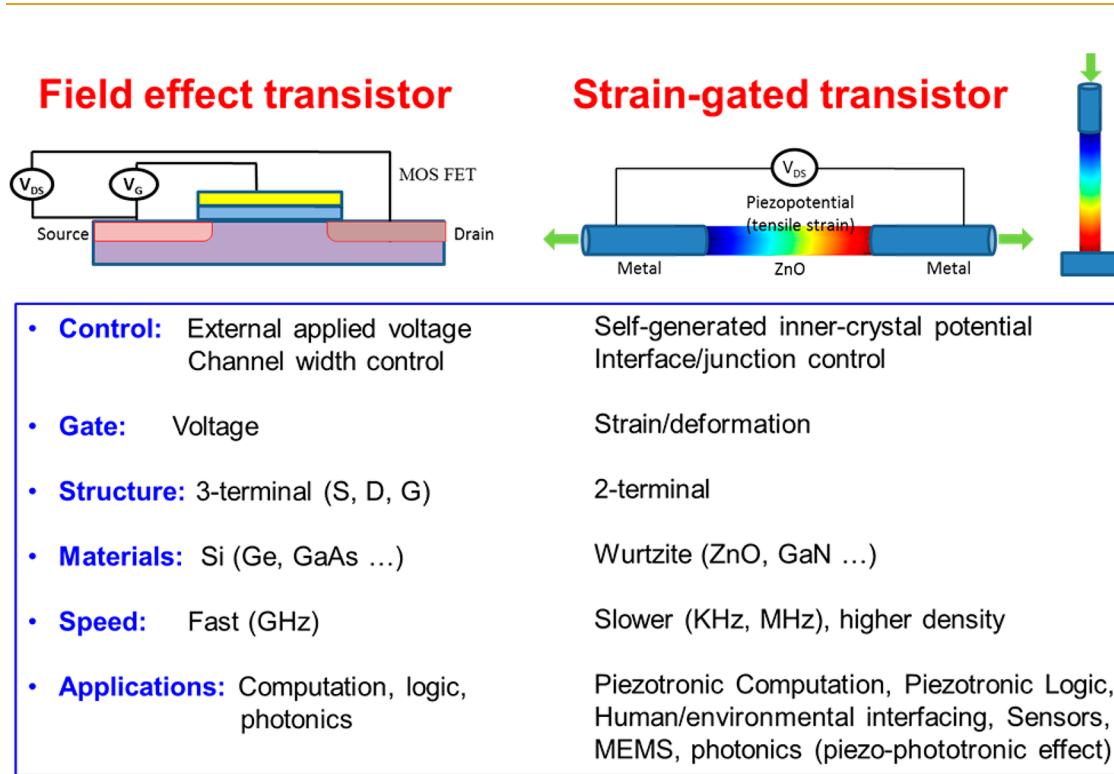


Figure 5. Comparison between traditional FET and strain-gated transistor (SGT).

TABLE 1. Comparison between Piezoresistive Effect and Piezotronic Effect

piezoresistive effect	piezotronic effect
linear $I-V$ curve	nonlinear "rectifying" $I-V$ curve
symmetric effect on end contacts	asymmetric effect on end contacts
no polarity	strong polarity
"volume" effect	"interface" effect
no switch function	switch function

CARRY and SUM, are plotted in blue and red lines, respectively, as shown in Figure 4b. The corresponding experimental truth table (with the physical values and logic levels of input and output signals) of the piezotronic strain-gated half-adder is presented in Figure 4c, which confirms clearly that the piezotronic strain-gated half-adder performs the one-bit binary addition over input mechanical strains and provides corresponding computation results in the electrical domain. As demonstrated by the above strain-gated logic operations, in contrary to traditional FET, the two-terminal strain-gated piezotronic SGTs process/interface mechanical strain input directly with the electrical controlling output signals under the influence of the self-generated inner-crystal potential (piezopotential).

A comparison between SGT and traditional FET is presented in Figure 5 and Table 1.

CONCLUSION

In summary, by using the piezoelectric polarization charges created at the metal–GaN NB interface under strain to modulate transport of local charge carriers across the Schottky barrier, the piezotronic effect has been utilized to convert mechanical stimuli applied on wurtzite-structured GaN NB into electronic controlling signals, based on which GaN NB strain-gated transistors (SGTs) have been fabricated. By further assembling and integrating GaN NB SGTs, universal logic devices such as NOT, AND, OR, NAND, NOR, and XOR gates have been demonstrated for performing mechanical–electrical coupled piezotronic logic operations. Moreover, basic piezotronic arithmetic operation such as one-bit binary addition by half-adder has been implemented to perform computations over mechanical signals and provide corresponding electrical output results. The demonstrated concept of strain-gated piezotronic logic operation/computation may find applications in human–machine interfacing, MEMS, biomedical diagnosis/therapy, and prosthetics.

EXPERIMENTAL SECTION

GaN NB Synthesis and Characterization. GaN NBs were fabricated via the method called strain-controlled cracking of thin solid films.²⁷ The as-fabricated GaN NBs were characterized by SEM

(LEO FESEM 1550 and LEO FESEM 1530), TEM (JEOL-JEM 4000) with SAD, and HRTEM (FEI F30) with EDX.

GaN NB Piezotronic Transistor Fabrication. The device was fabricated by transferring and bonding an individual GaN NB laterally onto the polystyrene (PS) substrate, with its *c*-axis in

the plane of the substrate pointing to the drain. Silver paste was used to fix the two ends of the NB, serving as source and drain electrodes, respectively. Finally, a thin layer of polydimethylsiloxane was used to package the device, in order to not only enhance the adhesion of the silver paste to the PS substrate but also prevent the GaN NB from contamination or corrosion by gases or liquid.

Experimental Setup for Piezotronic Logic Devices and Digital Circuit. A function generator (model no. DS345, Stanford Research Systems, Inc.) and a low-noise voltage preamplifier (model no. SR560, Stanford Research Systems, Inc.) were used for electrical measurements. One end of the device was fixed tightly on a sample holder with the other end free to be mechanically bent. The tensile and compressive strains were introduced by using a three-dimensional mechanical stage with a movement resolution of 1 μm . The performances of the device under different strains were measured by a computer-controlled measurement system.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: More detailed information about current-strain transfer characteristic of GaN NB piezotronic transistor, schematics, experimental truth table, and measured output voltages of piezotronic AND gate, OR gate, and XOR gate. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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